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Q75858
1 of 1
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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02360224.6

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

DEN HAAG, DEN
THE HAGUE, 14/08/02
LA HAYE, LE

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.:
Demande n°: 02360224.6

Anmeldetag:
Date of filing:
Date de dépôt: 26/07/02

Anmelder:
Applicant(s):
Demandeur(s):
ALCATEL
75008 Paris
FRANCE

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
A fast sample-and-hold peak detector circuit

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
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Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing:
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Bemerkungen:
Remarks:
Remarques:

A FAST SAMPLE-AND-HOLD PEAK DETECTOR CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to circuitry for detecting peak levels of signals and particularly fast sample-and-hold peak detectors for analyzing signals of generally arbitrary wave shape and form having a high precision, high slew-rate, very short retention, and a low distortion.

Background

Peak signal detectors are widely known and useful circuit devices. A peak detector may be used in an analog-to-digital signal converter, as a demodulator, or as a diagnostic tool. Various circuit solutions have been suggested for providing peak signal indications. Among them are peak envelope detectors, sample-and-hold peak detector circuits and level sensing circuits. Known solutions have a wide variety of limitations and disadvantages, including limitations on large amplitude operating range and frequency range and inability to approach true peak level detection.

What is needed is a peak detector which approaches true peak detection over a wide frequency range with high precision, high slew-rate, very short retention, and a low distortion.

A technique of detecting an analog signal at high speed and converting it into a digital signal has recently been essential to networking and multimedia. There a sample-and-hold peak detector circuit is necessary for an analog-to-digital conversion. As one method of the sample-and-hold peak detector circuit, there is a combination of a high-speed switch circuit and a voltage holding capacitor, for catching analog signals sampled in a short time slot and holding their peak values.

For circuits processing digital signals only, and circuit for optical telecommunications and optical interconnects, for signal readout circuits for a magnetic memory and semiconductor memory, and the like, the input signal levels of which are varied and unclear, for all these circuits, it is important that an input signal level of the preamplifier is detected automatically

to determine the optimum operation point and minimize a distortion of waveform of a reproduced pulse.

In order to minimize the distortion, an automatic discrimination type waveform reproduction circuit has been employed which detects and normalizes a peak level of an input pulse signal to always discriminate the pulse signal by half the amplitude of the pulse signal irrespective of variations in the level of the input pulse signal.

Peak detectors are also used for signal surveillance. For instance, input loss of signal (ILOS) detection is crucial for a wide range of devices. Here a peak detector is used to indicate whether a signal is absent by detecting no peaks.

It is a sample-and-hold peak detector circuit that is important in common to the foregoing examples. In particular, it is desirable for a circuit for processing a signal with an arbitrary pattern, such as the optical interconnection, to respond to a burst waveform and it is important to respond at high speed of not less than nanoseconds in order to correctly detect and hold a peak value of the first-input pulse. Recently there have been great demands that the sample-and-hold peak detector circuit should be relatively small in size or compact so as to be incorporated into an IC without any external capacitor. Also there have been demands for low power consumption in order to incorporate the sample-and-hold peak detector circuit into a multi-channel array, as well as a demand for a compensation of the technology dependent charging and discharging current. A further demand is the technology independence as well as the temperature and power supply independence of the sample-and-hold characteristics.

In US Patent No. 5,986,481 Kaminshi describes the fundamental arrangements of known prior art sample-and-hold peak detector circuits, illustrated in Fig. 1 and Fig. 2. The operation principle of each circuit is as follows. In the circuit of Fig. 1, a pulse input to an input terminal of a differential amplifier constituted of transistors T1 and T2, is compared with an output voltage of the sample-and-hold peak detector circuit and, if the voltage of the input pulse is higher than the output voltage with respect to Vee, an error is amplified and the base voltage of a switching transistor T3 is increased. Transistor T3 is turned on to start discharging a voltage holding capacitor C1. When the output voltage of the emitter follower circuit of a transistor T4 reaches the voltage of the input peak, the base voltage of the transistor T3 is lowered to cut off the current flowing into the transistor T3. If the top voltage of the input

pulse is maintained until the current is cut off the voltage with which the voltage holding capacitor C1 is discharged, becomes equal to the peak voltage of the input pulse.

Since the leak peak current of the transistor T4 is low, the time constant of charging of the capacitor is large and its peak voltage is maintained.

The operation of the switching transistor T3 will be described in more detail. The transistor T3 is a bipolar transistor and thus has a characteristic of causing a current to flow exponentially with respect to a base-to-emitter voltage. When the amplitude of base-to-emitter voltage is small, the dynamic impedance is high, the injected current is small, and the peak transit time is long. On the other hand, when the amplitude exceeds a certain value, the impedance is drastically lowered and the charging time is too short, with the result that a feedback is delayed and so is the cutoff of the switching transistor, thus causing an overshoot of the output voltage.

Consequently, an input voltage range for normally operating the circuit is restricted, and it is difficult to widen an input dynamic range. If the input voltage is too high, a collector current may flow through the transistors beyond a tolerable range, and the cutoff frequency may decrease, thereby causing a delay in response.

A circuit capable of excluding the above drawbacks to some extent, is shown in Fig. 2. In the circuit of Fig. 2, the voltage holding capacitor C1 is charged with a current which is almost proportional to the amplitude of an error voltage by a current output amplifier using a PNP transistor in place of a switch of an NPN transistor (shown in Fig. 1) with drastically changing impedance. In the circuit of Fig. 2, a power supply voltage needs to be higher than that of the circuit of Fig. 1 and the PNP transistor should satisfy a high speed operation.

In general, however, the bandwidth of the PNP transistor is about one-tenth of that of the NPN transistor; thus, the circuit of Fig. 2 has an essential problem that a high-speed operation cannot be satisfied.

The problem of the circuit shown in Fig. 1 on principle is an exponentially, nonlinear response to an input voltage of a switching transistor. However, this problem can be resolved if, as in the circuit of Fig. 2, the NPN switching transistor is operated so as to exhibit a linear response to the input voltage.

A high gain feedback amplifier may be useful for the sample-and-hold peak detector circuit in order to linearly operate an element originally having a remarkably nonlinear characteristic. In this case, usually, there occurs a problem that a high-speed operation cannot be carried out due to a delay in a high gain feedback as well as a problem that a large-sized circuit increases in chip area and thus in power consumption.

BRIEF DESCRIPTION OF THE INVENTION

The invention is based on the idea of definable matching characteristics, i.e. definable time parameter via discharge current compensation and defined constant current sources.

The circuit according to the invention consists of four coupled parts: a comparator circuit, a sample and hold circuit, a compensation circuit, and an unload circuit.

The circuitry for generating an output signal representative of peak level signals over a wide frequency range according to the invention comprises a comparator circuit at a first control input to receive an arbitrary input signal and providing a fixed reference signal for comparison with a varying signal across a charge stored in a sample and hold circuit. The circuitry further comprises a switch coupled to the comparator for controlling a first current for charging the sample and hold circuit, and a compensation circuit for compensation of defect currents. Furthermore the circuitry comprises an unload circuit for allowing controlling the de-charging characteristic.

OBJECTS AND ADVANTAGES OF THE INVENTION

The invention is a **Sample-and-Hold Peak Detector Circuitry** comprising a comparator circuit comprising two signal inputs and a signal output, where the output signal depends from the difference between the input signals, a sample and hold circuit comprising switching means controlled by said signal output for sampling and holding means (Chold) for holding the output signal, a compensation circuit for compensating defect currents comprising emulating means for emulating defect currents caused by said comparator circuit influencing

the functionality of said sample and hold circuit, and an unload circuit comprising a clearing means for decreasing the output signal (Vpeak) of said sample and hold circuit.

The compensation circuit might comprising a current mirror circuit mirroring defect currents emulated by said emulating means. And it might comprising copies of parts of the comparator circuit as emulating means.

The unload circuit might comprising a constant current source. This constant current source might be an adjustable constant current source. And it might be realized by multiple switchable constant current sources. The switchable constant current sources might be switchable by transfer gates.

The comparator circuit is implemented in differential logic. And the comparator circuit comprising of an current switch and a constant current source. The differential logic is differential emitter coupled logic.

Accordingly, it is an object and advantage of the present invention to provide a particularly fast sample-and-hold peak detector for analyzing signals of generally arbitrary wave shape and form having a high precision, high slew-rate, very short retention, and a low distortion.

These and other objects and advantages of the present invention will become apparent to those of ordinary skill in the art from a consideration of the drawings and ensuing description.

BRIEF DESCRIPTION OF THE FIGURES

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

Fig. 1 is a circuit diagram showing an example of a prior art sample-and-hold peak detector circuit;

Fig. 2 is a circuit diagram showing another example of the prior art sample-and-hold peak detector circuit;

Fig. 3 is a circuit diagram illustrating a sample-and-hold peak detector circuit of the present invention;

Fig. 4 is a circuit diagram illustrating an example of a sample-and-hold peak detector circuit according the present invention;

Fig. 5 is a diagram showing the output voltage of a sample-and-hold peak detector circuit with a large hold time according to the present invention;

Fig. 6 is a diagram showing the output voltage of a sample-and-hold peak detector circuit with a small hold time according to the present invention;

DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons from an examination of the within disclosure.

Fig. 3 shows principle circuit diagram of a sample-and-hold peak detector according to the invention. The diagram consists of four parts: a comparator 'Comparator circuit', a sample-and-hold circuit 'Sample&Hold circuit', a compensation circuit 'Compensation circuit', and an unload circuit 'Unload circuit'.

The comparator 'Comparator circuit' consists of an current switch implemented with two bipolar transistors Q1 and Q2, two resistors R1 and R2, and a constant current source I0.

The sample-and-hold circuit 'Sample&Hold circuit' consists of a charging current source I1, an electronic switch SW, as well as a capacity Chold.

The compensation circuit 'Compensation circuit' consists of a current mirror implemented with two positive channel Field Effect Transistors (pFETs) P1 and P2, as well as a bipolar transistor Q6, and a constant current source I2 serving half of the current of I0.

The unload circuit 'Unload circuit' consists of multiple constant current sources for determining the de-charging current of the capacity.

The 'Comparator circuit' building a voltage comparator, comparing the input signal voltage Vin with the output signal voltage Vpeak. Supposing the capacity Chold is uncharged. If Vin is greater than Vpeak, the electronic switch SW will be closed. This has the effect that the capacity Chold will be loaded by a switchable current source I1, and the potential at the output will increase, the comparator will detect if Vpeak has reached Vin and shall release the electronic switch SW. The voltage Vpeak remains stored by the capacity Chold. The procedure iterates if, Vin is greater than Vpeak.

The characteristic for unloading of the hold voltage Vpeak (in case of an open electronic switch SW) is determined by the base current of transistor Q2 and the capacity Chold.

The 'Compensation circuit' has the functionality to compensate the base current of transistor Q2 de-charging the capacity Chold. Therefore, the base current of transistor Q6 is mirrored by the transistors P1 and P2 for charging the capacity Chold. The current through P2 is identical with the base current of transistor Q6 over the transistor P1, if P1 and P2 are identical as well as if Q2 and Q6 are identical, and the constant current source I2 serves the halve of the current of I0. This compensation is necessary because otherwise the base current of Q2 will uncontrolled unload the capacity Chold inhibit to define an exact de-charging time.

The 'Unload circuit' determines exactly the de-charging of the capacity Chold by the constant current source I3, serving currents Iconst(1..n).

Fig. 4 shows a detailed circuit diagram of a sample-and-hold peak detector according to the invention. The four parts of the principal circuit diagram: 'Comparator circuit', 'Sample&Hold circuit', 'Compensation circuit', and 'Unload circuit' are detailed.

The 'Comparator Circuit' consists of a two-stage bipolar amplifier to ensure the comparator functionality. This has the effect of high precision and low overshoot. The first stage is realized by the transistors Q1 and Q2 and the collector resistors R1 and R2. Transistor Q10 and resistor R10 are designed to be the current source of the amplifier. The second stage consists of the transistors Q7 and Q8 and the collector resistors R2 and R4. Transistor Q15 and Resistor R15 are forming the current source of the second stage. Both amplifier stages are coupled via emitter-followers. A first emitter-follower pair consists of the transistors Q3 and Q4 with the current sources implemented by the transistors Q11 with resistor R11 and

transistor Q12 with resistor R11. A second emitter-follower pair consists of the transistors Q5 and Q6 as well as the corresponding current sources, formed by transistor Q13 and resistor R13 as well as transistor Q14 and resistor R14.

The 'Sample&Hold circuit' comprises a transistor Q9 and the capacity Chold. Transistor Q9 works as a switch triggered by the output voltage of the 'Comparator circuit' (collector of Q7). By using a bipolar transistor a high slew rate is achieved.

The 'Compensation circuit' is realized by a current mirror P1 and P2 as well as the bipolar transistor Q2D having a current source Q10D with R10D. The current source has half of the value of the current source Q10 with R10. This ensures that the capacity Chold is charged with the current flowing of through the basis of transistor Q2.

The 'Unload circuit' comprises multiple current sources Q23 with R23, Q22 with R22, Q21 with R 21, and Q20 with R20. The current sources are defined by a reference current Iref unloading well defined the capacity Chold. The switches for selecting the unloading current might be implemented by transfer gate switches.

Fig. 5 shows the output voltage of a sample-and-hold peak detector circuit according to the present invention with a large hold time; realized by a small de-charging current. The peak detector reaches within c.a. 7ns the peak value of the input signal and holds this value for further 10ns even without new input.

Fig. 6 shows the output voltage of a sample-and-hold peak detector circuit according to the present invention with a large hold time; realized by a large de-charging current. The peak detector reaches within c.a. 7ns the peak value of the input signal but the output voltage is decreasing now immediately. After further 10ns the output voltage has decreased from 3.42V below 3.40V.

Alternative Embodiments

Although illustrative presently preferred embodiments and applications of this invention are shown and described herein, many variations and modifications are possible which remain within the concept, scope, and spirit of the invention, and these variations would become clear to those of skill in the art after perusal of this application.

For example, the invention can be used with any type of transistor technology and semiconductor technology. The invention, therefore, is not intended to be limited except in the spirit of the appended claims.

CLAIMS

What is claimed is:

1. A **Sample-and-Hold Peak Detector Circuitry** comprising
   - a comparator circuit (Comparator Circuit) comprising two signal inputs (Vin, Vpeak) and a signal output (SW), where the output signal depends from the difference between the input signals,
   - a sample and hold circuit (Sample&Hold Circuit) comprising switching means (SW) controlled by said signal output for sampling and holding means (Chold) for holding the output signal (Vpeak),
   - a compensation circuit (Compensation Circuit) for compensating defect currents comprising emulating means (Fig. 3 Q6, I2; Fig. 4 Q2D, Q10D, R10D) for emulating defect currents caused by said comparator circuit (Comparator Circuit) influencing the functionality of said sample and hold circuit (Sample&Hold Circuit), and
   - an unload circuit (Unload Circuit) comprising a clearing means (Fig. 3 I3; Fig. 4 Q20, Q21, Q22, Q23, R20, R21, R22, R23) for decreasing the output signal (Vpeak) of said sample and hold circuit.

2 The **Circuitry** according to claim 1 where said compensation circuit (Compensation Circuit) comprising a current mirror circuit (Fig. 3,4 P1, P2) mirroring defect currents emulated by said emulating means (Fig. 4 Q2D, Q10D, R10D) .

3. The **Circuitry** according to claim 1 where said compensation circuit (Compensation Circuit) comprising copies of parts (Fig. 3 Q2, I0; Fig. 4 Q2, Q10, R10) of the comparator circuit (Comparator Circuit) as emulating means (Fig. 3 Q6, I2Fig. 4 Q2D, Q10D, R10D).

4. The **Circuitry** according to claim 1 where said unload circuit (Unload Circuit) comprising a constant current source (Fig. 3 I3, Fig. 4 Q20, Q21, Q22, Q23, R20, R21, R22, R23).

5. The **Circuitry** according to claim 4 where said constant current source is an adjustable constant current source (Fig. 4 Q20, Q21, Q22, Q23, R20, R21, R22, R23, Iref).

6. The **Circuitry** according to claim 5 where said adjustable constant current source is realized by multiple switchable constant current sources (Fig. 4 Q20, Q21, Q22, Q23, R20, R21, R22, R23).

7. The **Circuitry** according to claim 6 where said switchable constant current sources (Fig. 4 Q20, Q21, Q22, Q23, R20, R21, R22, R23) are switchable by transfer gates.

8. The **Circuitry** according to claim 1 where said comparator circuit (Comparator Circuit) is implemented in differential logic.

9. The **Circuitry** according to claim 1 where said comparator circuit (Comparator Circuit) comprising of an current switch (Fig. 4 Q1, Q2) and a constant current source (Fig. 4 Q10, R10).

10. The **Circuitry** according to claim 8 where said differential logic is differential emitter coupled logic.

ABSTRACT

This invention relates to circuitry for detecting peak levels of signals and particularly fast hold and sample peak detectors for analyzing signals of generally arbitrary wave shape and form having a high precision, high slew-rate, very short retention, and a low distortion. The Circuitry comprising a comparator circuit (Comparator Circuit) comprising two signal inputs and a signal output, where the output signal (Vpeak) depends from the difference between the input signals (Vin, Vpeak), a sample and hold circuit (Sample&Hold Circuit) comprising switching means (SW) controlled by said signal output for sampling and holding means (Chold) for holding the output signal (Vpeak), a compensation circuit (Compensation Circuit) for compensating defect currents comprising emulating means (Q6, I2) for emulating defect currents caused by said comparator circuit (Comparator Circuit) influencing the functionality of said sample and hold circuit (Sample&Hold Circuit), and an unload circuit (Unload Circuit) comprising a clearing means (I3) for decreasing the output signal (Vpeak) of said sample and hold circuit (Sample&Hold Circuit).

Figure 3.

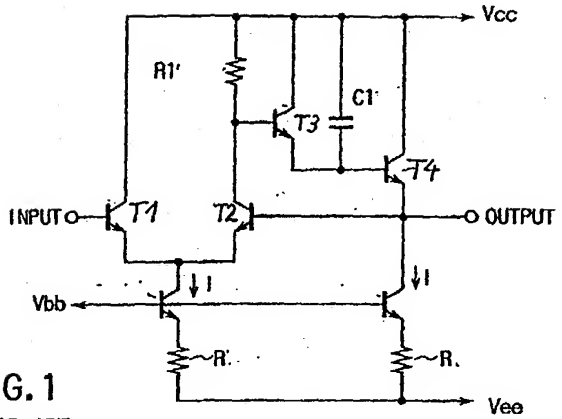

FIG. 1
PRIOR ART

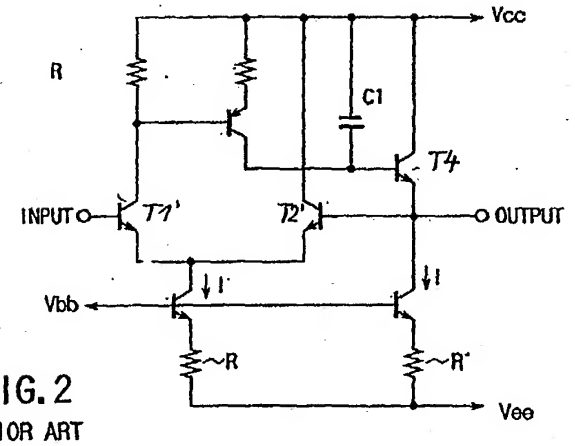

FIG. 2
PRIOR ART

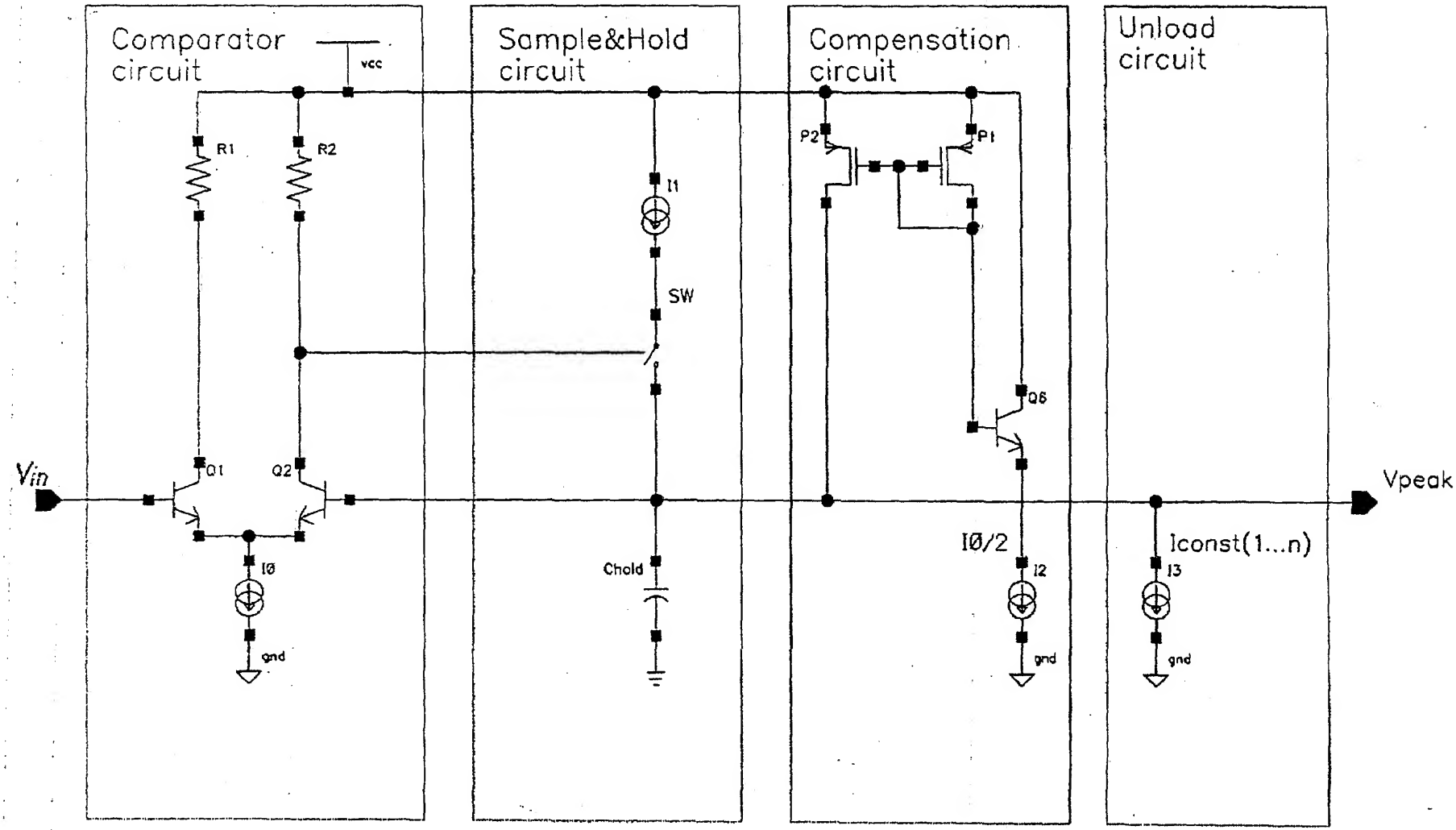
Comparator circuit
vcc
R1
R2
Q1
Q2
Vin
I0
gnd
Sample&Hold circuit
I1
SW
Chold
Compensation circuit
P2
P1
Q6
I0/2
I2
gnd
Unload circuit
Iconst(1...n)
I3
gnd
Vpeak

FIG. 3

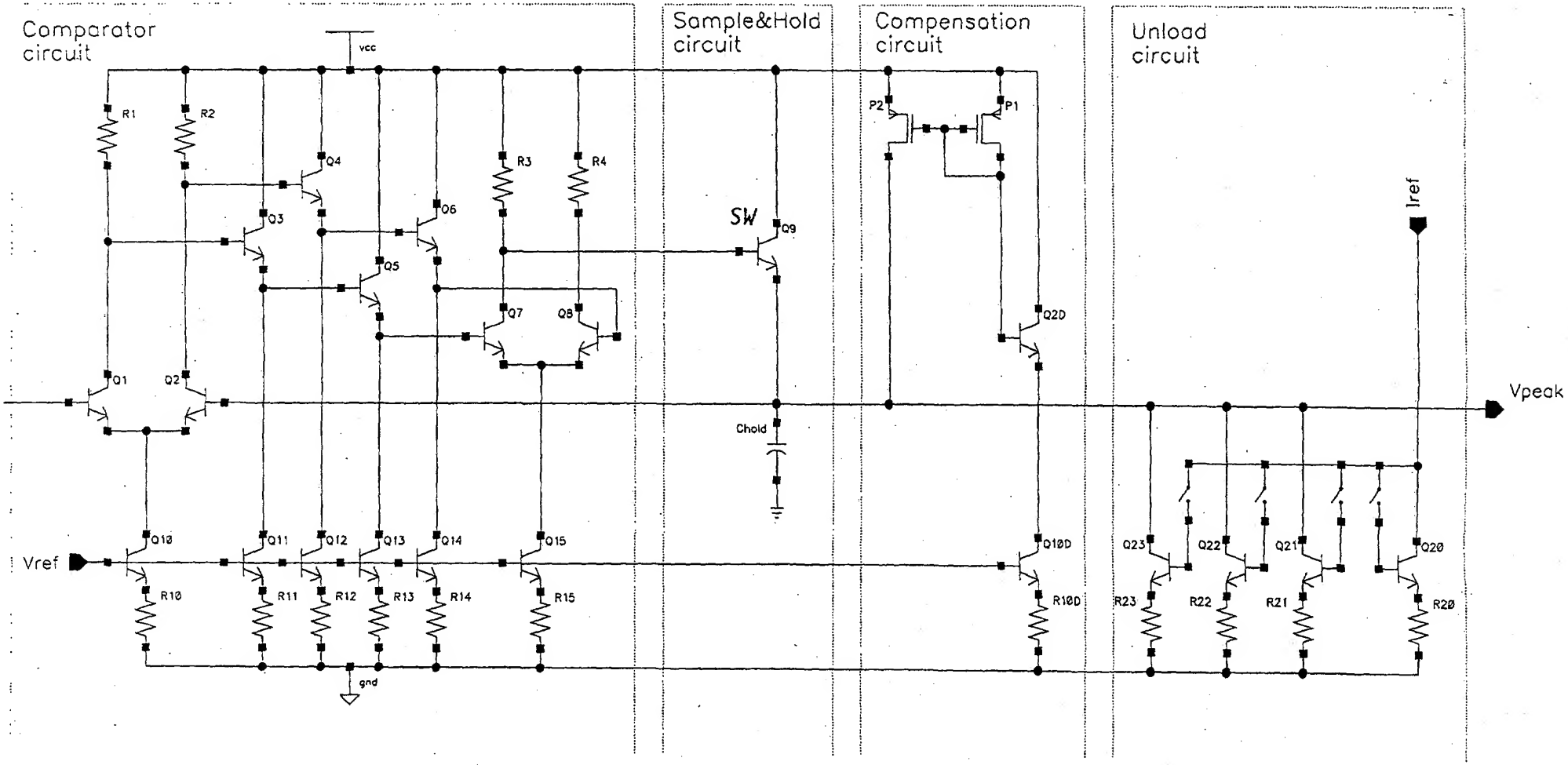
Comparator circuit
Sample&Hold circuit
Compensation circuit
Unload circuit
vcc
R1
R2
R3
R4
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
SW
Q9
P2
P1
Q2D
Iref
Vpeak
Chold
Vref
Q10
Q11
Q12
Q13
Q14
Q15
Q10D
R10
R11
R12
R13
R14
R15
R10D
Q23
Q22
Q21
Q20
R23
R22
R21
R20
gnd

FIG 4.

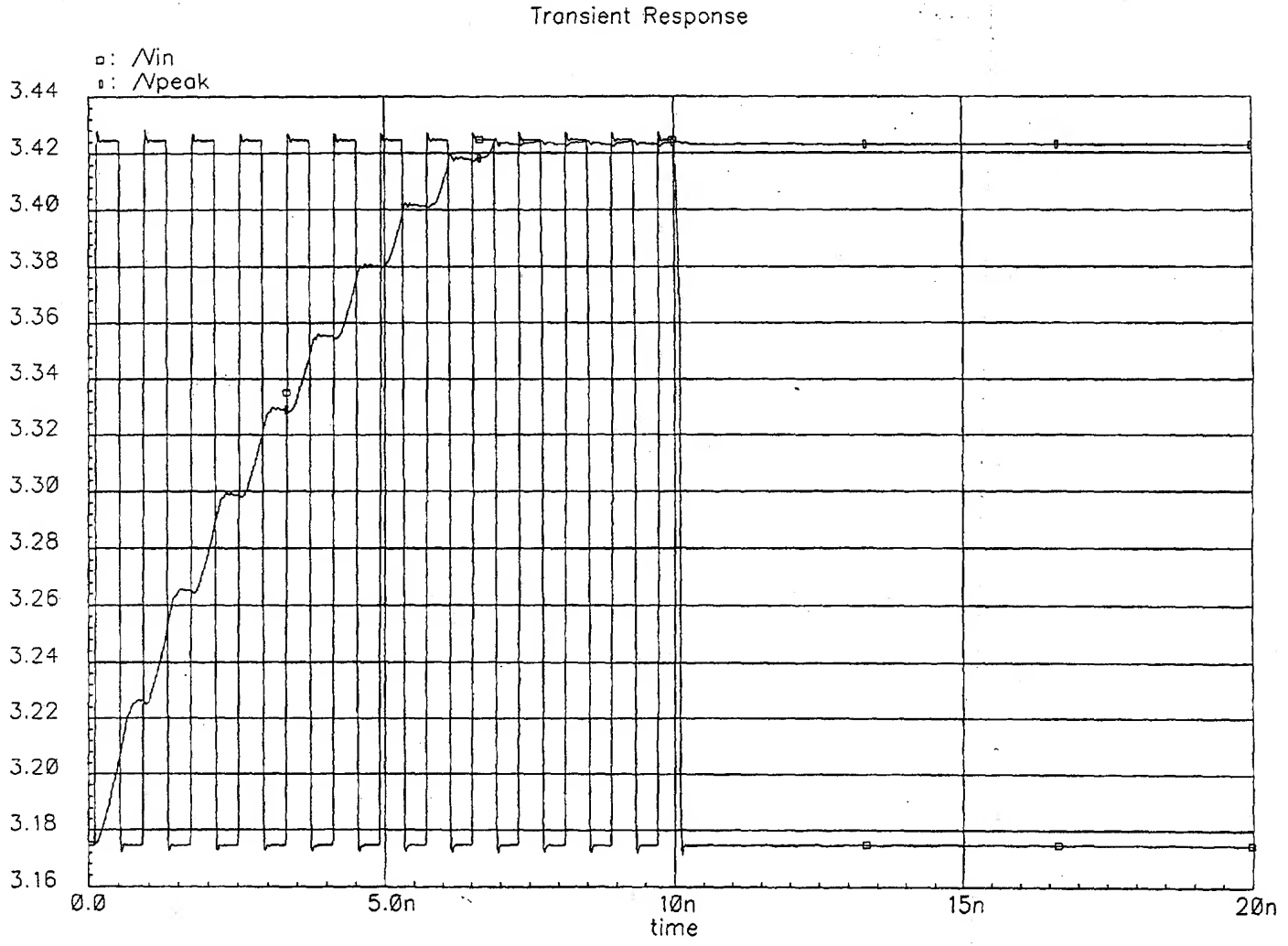
Transient Response
/Vin
/Vpeak
3.44
3.42
3.40
3.38
3.36
3.34
3.32
3.30
3.28
3.26
3.24
3.22
3.20
3.18
3.16
0.0
5.0n
10n
15n
20n
time

FIG. 5

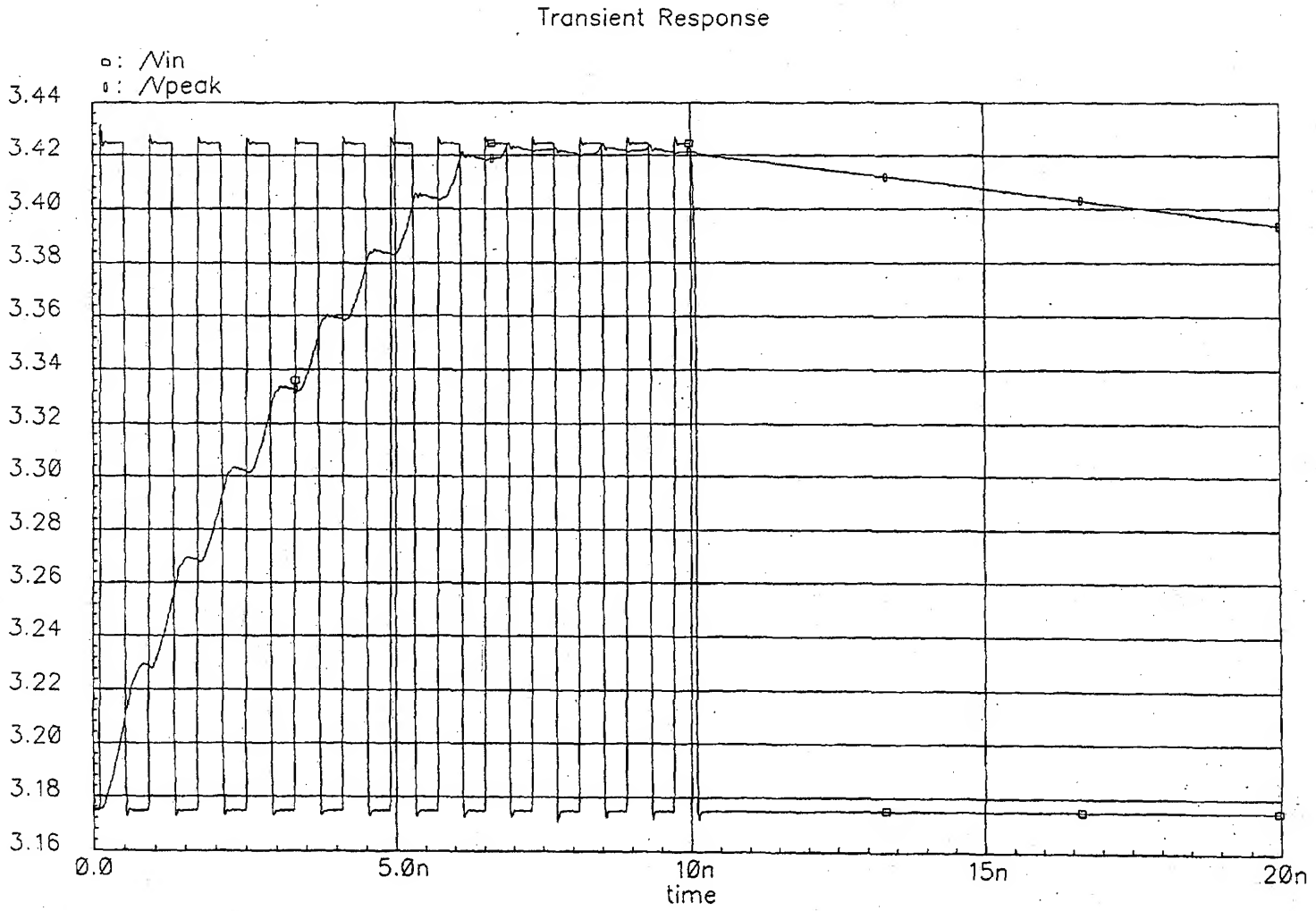
Transient Response
Vin
Vpeak
3.44
3.42
3.40
3.38
3.36
3.34
3.32
3.30
3.28
3.26
3.24
3.22
3.20
3.18
3.16
0.0
5.0n
10n
15n
20n
time

FIG. 6

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Eingang bei ZPL
09. JAN 2003
Term. Bearb. ~~10.03.03~~ MH

Datum/Date
10.01.03

Zeichen/Ref./Réf.	Anmeldung Nr./Application No./Demande n°./Patent Nr./Patent No./Brevet n°.
113 511	02360224.6-2206-

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire
ALCATEL

COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

☐ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

The following specifications given by the applicant have been approved by the Search Division:

☒ abstract ☒ title

☐ The abstract was modified by the Search Division and the definitive text is attached to this communication.

The following figure will be published together with the abstract: 3

REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 36 0224

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 986 481 A (KAMINISHI KATSUJI) 16 November 1999 (1999-11-16) * the whole document *	1-10 ✓	G11C27/02
X A	US 5 995 166 A (KAWANO TSUTOMU) 30 November 1999 (1999-11-30) * column 8, line 23 - column 17, line 4; figures 2,5 *	1,4,5,8,9 ✓ 2,3,6,7,10	
A	US 4 038 568 A (NASUTA JR ANTHONY T ET AL) 26 July 1977 (1977-07-26) * column 2, line 17 - column 4, line 10; figure 1 *	1-10 ✓	
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 01, 29 January 1999 (1999-01-29) & JP 10 267967 A (TOSHIBA CORP), 9 October 1998 (1998-10-09) * abstract *	1,3,8,9 ✓	
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 234 (P-230), 18 October 1983 (1983-10-18) & JP 58 122698 A (SONY KK), 21 July 1983 (1983-07-21) * abstract *	1-10 ✓	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	23 December 2002	Henderson, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 36 0224

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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23-12-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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